In the Specification:

Please amend paragraphs 16 and 51 as follows:

[0016] FIG. 4 is a cross-sectional view of ~~NFET~~300 NFET 300 that may be fabricated alone or simultaneously with the PFET 100 of FIG1 according to the present invention.

[0051] FIG. 4 is a cross-sectional view of NFET 300 that may be fabricated alone or simultaneously with PFET [[300]] 100 of FIG 1, according to the present invention. FIG. 4 is similar to FIG 1, except for several differences. First, single crystal region 110 is P-doped, instead of N-doped, source and drain regions 120A and 120B are N-doped instead of P-doped, single crystal regions 125A and bc are N-doped instead of P-doped, N-well 145 is replaced with a P-well 145. Second, structurally, only thick regions 215A and 215B of respective dielectric layers 130A and 130B, epitaxial layers 285A and 285B intervene between respective polysilicon source/drain regions 120A and 120B and silicon substrate 150 rather than respective thin regions 210A and 210B (see FIG. 1) of dielectric layers 130A and 130B, and epitaxial layers 285A and 285B extend under respective thick regions 215A and 215B of dielectric layers 130A and 130B. Source/drain dopant species from source 120A and drain 120B may or may not extend into respective epitaxial layers 285A and 285B.